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IN THE CLAIMS

Cancel claims 12-20 without prejudice

Claim 1 (currently amended): A method of forming an integrated circuit device including at least one semiconductor memory array region and logic circuits including a support region including the steps as follows:

[[form]] forming a thick ~~deposit of~~ polysilicon layer having a first thickness over [[in]] both [[the]] said array region where word lines are located and [[the]] over said support region where [[the]] said logic circuits are located;

then ~~remove the~~ removing said thick ~~layer of~~ polysilicon layer only [[in the]] from said array region;

then ~~deposit~~ depositing a thin ~~layer of~~ polysilicon layer over [[in]] both [[the]] said array region and [[the]] said support region, with said thin polysilicon layer having a second thickness substantially less than said first thickness, and with said thin polysilicon layer being formed on said thick polysilicon layer in said support region;

then ~~deposit~~ depositing a metallic conductor coating including at least an elemental metal layer portion over [[the]] said thin ~~layer of~~ polysilicon layer; and

then forming word lines in said array region from said thin polysilicon layer and forming gate electrodes ~~in the array region and~~ in said support region from said thick polysilicon layer and said thin polysilicon layer above said thick polysilicon layer. ~~respectively.~~

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Claim 2 (currently amended): [[The]] A method ~~of claim 1 wherein~~ of forming an integrated circuit device including at least one semiconductor memory array region and logic circuits including a support region including the steps as follows:

~~the method begins with formation of~~ forming a sacrificial polysilicon layer over [[the]] said array region followed by formation of a gate oxide layer over [[the]] said device; [[, and]]

forming a thick polysilicon layer in both said array region where word lines are located and said support region where the logic circuits are located;

removing said thick polysilicon layer only over the array region and removing the sacrificial polysilicon layer;

then precleaning the device;

~~performing the step of precleaning the device prior to the~~ then depositing ~~deposit of the~~ a thin ~~layer of~~ polysilicon layer in both said array region and said support region,

then depositing a metallic conductor coating including at least an elemental metal layer portion over said thin polysilicon layer; and

then forming word lines and gate electrodes in said array region and in said support region respectively.

Claim 3 (currently amended): The method of claim 2 including forming a barrier layer between [[the]] said thin ~~layer of~~ polysilicon layer and [[the]] said metal layer.

Claim 4 (currently amended): The method of claim 1 wherein [[the]] said thin ~~layer of~~ polysilicon layer comprises amorphous silicon.

Claim 5 (currently amended): The method of claim 4 wherein the method begins with ~~formation~~ forming of a blanket sacrificial polysilicon layer over [[the]] said array region followed by ~~formation~~ forming of a blanket gate oxide layer over [[the]] said device.

Claim 6 (currently amended): The method of claim 5 including forming a barrier layer between [[the]] said thin ~~layer of~~ polysilicon layer and [[the]] said metallic conductor coating.

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Claim 7 (currently amended): The method of claim 2 wherein a gate oxide layer is formed over [[the]] said device after formation of [[the]] said sacrificial polysilicon layer.

Claim 8 (currently amended): The method of claim 4 ~~wherein~~ including forming a gate oxide layer ~~is formed~~ over the device after formation of the sacrificial polysilicon layer.

Claim 9 (currently amended): The method of claim 1 ~~wherein~~ including forming a capping silicon nitride layer ~~is formed~~ over [[the]] said metal layer before forming word lines and gate electrodes in [[the]] said array region and in said support region.

Claim 10 (currently amended): The method of claim 9 including:

forming [[the]] said integrated circuit device on a semiconductor substrate with a polysilicon stud [[is]] in a trench in [[the]] said semiconductor substrate under an electrically conductive word line with [[the]] said stud being electrically insulated from [[the]] said substrate by dielectric material on sidewalls of said trench and with an Array Top Oxide (ATO) layer formed above [[the]] said substrate aside from [[the]] said polysilicon stud; [[and]]

[[after]] forming word lines ~~and gate electrodes~~ in [[the]] said array region; [[and]]

forming gate electrodes in said support region; and

forming sidewall spacers on sidewalls thereof.

Claim 11 (currently amended): The method of claim 1 ~~wherein~~ including performing the step of precleaning ~~is performed~~ prior to the step of depositing [[the]] said thin ~~layer of~~ polysilicon layer in both [[the]] said array region and [[the]] said support region.

Claims 12-20 (canceled)

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Claim 21 (new): A method of forming an integrated circuit device including at least one semiconductor memory array region and logic circuits including a support region including the steps as follows:

forming a thick polysilicon layer having a first thickness of greater than or equal to 500Å over both said array region where word lines are located and over said support region where said logic circuits are located;

then removing said thick polysilicon layer only from said array region;

then depositing a thin polysilicon layer over both said array region and over said support region, said thin polysilicon layer having a second thickness of less than or equal to 300Å;

then depositing a metallic conductor coating including at least an elemental metal layer portion over said thin polysilicon layer; and

then forming word lines in said array region from said thin polysilicon layer and forming gate electrodes in said support region from said thick polysilicon layer and said thin polysilicon layer thereabove.

Claim 22 (new): The method of claim 21 including forming a sacrificial polysilicon layer over the array region prior to formation of said thick polysilicon layer.

Claim 23 (new): The method of claim 21 including forming a barrier layer between said thin polysilicon layer and said metal layer.

Claim 24 (new): The method of claim 21 wherein said thin polysilicon layer comprises amorphous silicon.

Claim 25 (new): The method of claim 24 beginning with forming of a blanket sacrificial polysilicon layer over said array region followed by forming of a blanket gate oxide layer over said device.

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Claim 26 (new): The method of claim 25 including forming a barrier layer between said thin polysilicon layer and said metallic conductor coating.

Claim 27 (new): The method of claim 21 including performing a precleaning step prior to the step of depositing said thin polysilicon layer in both said array region and said support region.

Claim 28 (new): The method of claim 27 including performing a second precleaning step prior to the step of depositing said metallic conductor coating over said thin polysilicon layer.

Claim 29 (new): The method of claim 28 wherein formation of said metallic conductor coating over said thin polysilicon layer comprises

seasoning said thin polysilicon layer with titanium atoms after said second precleaning step;

depositing a tungsten nitride (WN) with a thickness from about 40Å to about 150Å; and then depositing a tungsten (W) with a thickness from about 300Å to about 500Å thereabove.